AMENDMENTS TO THE SPECIFICATION

Please amend the specification, as follows:

Replace paragraph [0001] with the following amended paragraph [0001]:

This application claims priority from [[to]] Korean Patent Application No. 10-2003-0008010, filed on February 8, 2003, in the Korean Intellectual Property Office (KIPO), the entire contents of which are incorporated herein by reference ~~in its entirety~~.

Replace paragraph [0003] with the following amended paragraph [0003]:

Molding processes are typically used for sealing semiconductor chips after wire-bonding has been completed, by encapsulating the chips and the bonding wires with a chemical resin. The molding process is typically performed in a mold die, which is incorporated into a larger ~~apparatus~~ molding apparatus. A typical mold die comprises a pot for holding the mold resin, a cavity block for defining one or more cavities, a paddle, a runner block, and a gate block for defining and controlling a gate through which the resin may enter a cavity. A typical molding apparatus may include 2, 4, 6, or more separate cavity blocks [[are]] symmetrically disposed in a mold die and connected to a common pot through one or more runner blocks and gate blocks.

Replace paragraph [0004] with the following amended paragraph [0004]:

Molding processes can be broadly categorized into [[a]] single molding processes and [[a]] chip-array molding processes, depending on the number of semiconductor chips loaded in one cavity block. While only a single semiconductor chip is loaded in each cavity in a single molding process, a plurality of semiconductor chips are loaded to form a matrix in each cavity in a chip-array molding process. Since a chip-array molding process typically requires a greater amount of mold resin than a single molding process, the mold die gate for single molding processes may be relatively narrow, while the mold die gate for chip-array molding process will tend to be considerably wider to increase the rate at which the mold resin enters the cavity.

Replace paragraph [0008] with the following amended paragraph [0008]:

A recessed surface is provided in the cavity block 100 to define the cavity 105 that will be filled with mold resin that flows from the pot, through the runner block and through the gate 115 during the molding process. A plurality of semiconductor chips 12 on which the wire-bonding process has been completed may be arranged in cavity 105. The semiconductor chips 12 may be attached to, for example, a printed circuit board (PCB) [[10]] or other suitable substrate 10. In a typical mold die for molding a chip array, a regular array of, for example, four, six, or nine[[,]] semiconductor chips are attached [[to]] and wire-bonded to a printed circuit ~~substrate~~ board 10 using conventional assembly processes before being placed in the cavity 105.

Replace paragraph [0015] with the following amended paragraph [0015]:

Unlike cases in which the sweeping forces are applied in only one direction, the chip-array molding process must typically be carried out with sweeping forces applied in a plurality of directions while still accommodating demanding requirements for the positioning of bonding wires, the pitch between adjacent bonding wires, and the like. As described above with regard to FIG. 3, the mold resin flowing along both sides of the semiconductor chip 12 will tend to meet behind the rear side of the semiconductor chip 12. As a result, on the rear side of the semiconductor chip 12, bonding wires 20 on either side of region A are swept in opposite directions that tend to force the bonding wires toward each other.

Replace paragraph [0032] with the following amended paragraph [0032]:

Referring to [[FIGS]] FIGs. 4A-4C, cavities 205a, 205b, and 205c are arranged above a substrate 10 and are associated with gates 215a, 215b, and 215c, respectively, with the gates being ~~having~~ arranged in one corner of the cavities. The gates 215a, 215b, and 215c, that [[which]] control an opening through which mold resin may be injected into the corresponding cavity, have a predetermined width. Cavity blocks (not shown) for defining the cavities 205a, 205b, and 205c and gate blocks (not shown) for defining the gates 215a, 215b, and 215c may be constructed as a single element or may be assembled from multiple components to achieve the desired final configuration. The use of multiple components may also allow for the use of various materials having different properties for improving the performance, durability,

manufacturability, or other aspect of the blocks over that which could be achieved with a single integral block.